



TET ESTEL AS
ESTONIA

November
2015

Series
T333-400

Phase Control Press-Pack
Thyristor
Type T333-400

Center amplifying gate
Low on-state and switching losses
Designed for traction and industrial applications

Maximum mean on-state current	I_{TAV}	400 A			
Maximum repetitive peak off-state and reverse voltage	U_{DRM} U_{RRM}	1600 ÷ 2400 V			
Turn-off time	t_q	160; 200; 250; 320 μs			
U_{DRM}, U_{RRM}, V	1600	1800	2000	2200	2400
Voltage code	16	18	20	22	24
$T_{vj}, ^\circ C$	- 60 ÷ 125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	T333-400	Conditions
I_{TAV}	Mean on-state current	A	400 715	$T_c=93^\circ C$, $T_c=55^\circ C$, 180° half-sine wave, 50 Hz
I_{TRMS}	RMS on-state current	A	628	$T_c=93^\circ C$
I_{TSM}	Surge on-state current	kA	8,0 9,0	$T_{vj}=125^\circ C$ $T_{vj}=25^\circ C$ tp=10 ms $U_R=0$
I^2t	Limiting load integral	kA^2s	320 405	$T_{vj}=125^\circ C$ $T_{vj}=25^\circ C$
U_{DRM}, U_{RRM}	Repetitive peak off-state and reverse voltage	V	1600÷2400	$T_j \min \leq T_{vj} \leq T_{jM}$ 180° half-sine wave, 50 Hz Gate open
U_{DSM}, U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	1700÷2500	$T_j \min \leq T_{vj} \leq T_{jM}$ 180° half-sine wave tp=10 ms, Single pulse Gate open
(di _T /dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/ μ s	320 160	$T_{vj}=125^\circ C$; $U_D=0,67 U_{DRM}$, Gate pulse : 10V,5 Ω , 1 μ s rise time, 10 μ s
U_{RGM}	Peak reverse gate voltage	V	5	$T_j \min \leq T_{vj} \leq T_{jM}$
T_{stg}	Storage temperature	$^\circ C$	-60÷80	
T_{vj}	Junction temperature	$^\circ C$	-60÷125	

CHARACTERISTICS

U_{TM}	Peak on-state voltage	V	1,8	$T_{vj}=25^\circ C$, $I_{TM}=3,14 I_{TAV}$
$U_{T(TO)}$	Threshold voltage	V	1,1	$T_{vj}=125^\circ C$
R_T	On-state slope resistance	m Ω	0,6	1,57 $I_{TAV} < I_T < 4,71 I_{TAV}$
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	50 50	$T_{vj}=125^\circ C$, $U_D = U_{DRM}$ $U_R = U_{RRM}$

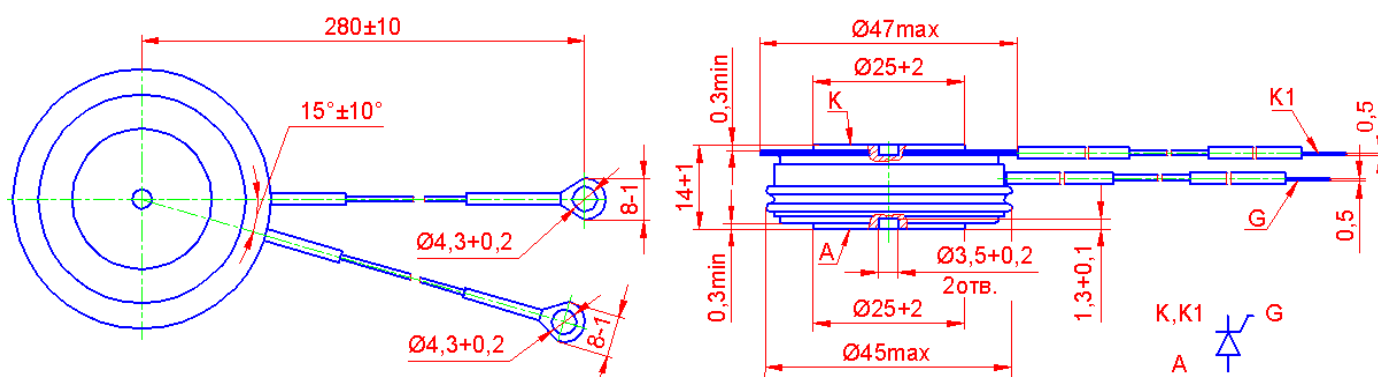
CHARACTERISTICS

Symbols and parameters		Units	T333-400	Conditions
I_L	Latching current	A	0,7	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$ Gate pulse : 10V, 5 Ω , 1 μs rise time, 10 μs
I_H	Holding current	A	0,5	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$, Gate open
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	$T_{vj}=25^{\circ}\text{C}$, $T_{vj}=-60^{\circ}\text{C}$ $U_D=12\text{V}$
I_{GT}	Gate trigger direct current	A	0,3 0,85	$T_{vj}=25^{\circ}\text{C}$, $T_{vj}=-60^{\circ}\text{C}$
U_{GD}	Gate non-trigger direct voltage	V	0,25	$T_{vj}=125^{\circ}\text{C}$, $U_D = 0,67 U_{DRM}$
I_{GD}	Gate non-trigger direct current	mA	10	Direct gate current
tgd	Delay time	μs	1,6	$T_{vj}=25^{\circ}\text{C}, U_D=500\text{V}$ $I_{TM} = 400 \text{ A}$
tgt	Turn-on time	μs	3,2	Gate pulse : 10V, 5 Ω , 1 μs rise time, 10 μs
tq	Turn-off time	μs	160÷320	$T_{vj}=125^{\circ}\text{C}$, $I_{TM}=400 \text{ A}$ $di_R/dt = 10 \text{ A}/\mu\text{s}$, $U_R=100\text{V}$ $U_D = 0,67 U_{DRM}$ $du_D/dt=50 \text{ V}/\mu\text{s}$
Qrr	Recovered charge	μC	1350	$T_{vj}=125^{\circ}\text{C}$, $I_{TM}=400 \text{ A}$ $di_R/dt = 10 \text{ A}/\mu\text{s}$, $U_R=100\text{V}$
trr	Reverse recovery time	μs	24	
Irrm	Peak reverse recovery current	A	110	
(du_D/dt)crit	Critical rate of rise of off-state voltage	V/ μs	500 1000	$T_{vj}=125^{\circ}\text{C}$, $U_D = 0,67 U_{DRM}$ Gate open
Rthjc	Thermal resistance junction to case	$^{\circ}\text{C}/\text{W}$	0,045	Direct current, double side cooled

ORDERING

	T	333	400	22	7	3	
	1	2	3	4	5	6	

1. Phase control thyristor.
2. Design version.
3. Mean on-state current, A.
4. Voltage code (22=2200 V).
5. Critical rate of rise of off-state voltage ($6 \geq 500 \text{ V}/\mu\text{s}$, $7 \geq 1000 \text{ V}/\mu\text{s}$).
6. Group of turn-off time ($du_D/dt=50 \text{ V}/\mu\text{s}$, $K2 \leq 320 \mu\text{s}$, $2 \leq 250 \mu\text{s}$, $P2 \leq 200 \mu\text{s}$, $3 \leq 160 \mu\text{s}$).



Mounting force : 9 ÷ 12 kN
Weight : 120 grams